REMARKS/ARGUMENTS

This Amendment is in response to the Final Office Action mailed March 2, 2004 and is being filed concurrently with a Request for Continued Examination. Consideration of the pending claims is respectfully requested.

A. §112 REJECTIONS

In the Office Action, claims 5-13 and 15-23 were rejected under 35 U.S.C. §112, first paragraph. It is alleged that there is no support in the specification for the encapsulant differing in composition from the thermal epoxy. With respect to claims 22-23, Applicants respectfully traverse the rejection because these claims do not include the "encapsulant composition" limitation noted above. With respect to claims 5-13 and 15-21, Applicants have removed this limitation has been removed from independent claims 5 and 9. Hence, Applicants respectfully request withdrawal of the 35 U.S.C. §112, first paragraph rejection.

Moreover, claims 5-13 and 15-23 were rejected under 35 U.S.C. §112, second paragraph for omitting the placement of the encapsulant with respect to other structures. With respect to claims 22-23, Applicants respectfully traverse the rejection because these claims do not include any limitations concerning encapsulant. With respect to claims 5-13 and 15-21, Applicants have amended claims 5 and 9 to identify that the encapsulant is applied over the integrated circuit, the thermal element and the thermal epoxy. Hence, Applicants respectfully request withdrawal of the 35 U.S.C. §112, second paragraph rejection.

B. §103(A) REJECTION

In the Office Action, claims 5-13 and 14-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jiang (U.S. Patent No. 5,208,519) in combination with Beane (U.S. Patent No. 6,003,586) and Fillion (6,306,680). Also, claims 19 and 21-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jiang in view of Beane, Fillion and AGEN (JP62-36091).

Applicants respectfully traverse the rejection because, *inter alia*, Jiang does not constitute prior art. Applicants submit herewith a declaration under 37 C.F.R. §1.131 signed by the inventors, Nagesh Vodrahalli and Biswajit Sur. The inventors declare that they conceived the claimed invention prior to August 31, 1999, the effective filing date of Jiang. A copy of the Intel Invention Disclosure pre-dating the August 31, 1999 filing date of Jiang is offered into evidence as Exhibit A. Reconsideration and withdrawal of this rejection is respectfully requested.

Moreover, as a side note, Applicants respectfully point out that claim 14 has been cancelled and presume that the inclusion of "claim 14" under the §103 rejection was a typographical error.

Conclusion

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 06/02/04

By _____
William W. Schaal
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12400 Wilshire Boulevard, Seventh Floor
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CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

☒ *deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.*

Date: 4/30/04

FACSIMILE

☐ *transmitted by facsimile to the Patent and Trademark Office.*

Susan McFarlane — *Date* 06/02/04

RESPONSE UNDER 37 CFR § 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	09/475,104	Confirmation No. 5963
Applicant	:	Nagesh Vodrahalli	
Filed	:	12/30/1999	
TC/A.U.	:	2827	
Examiner	:	James M. Mitchell	
Docket No.	:	042390.P6785	
Customer No.	:	8791	

DECLARATION UNDER 37 C.F.R. § 1.131

Assistant Commissioner for Patents
Washington, DC 20231-9999

Dear Sir:

We, Nagesh Vodrahalli and Biswajit Sur, hereby declare that:

1. We are joint inventors of the subject matter claimed in the above-identified patent application, which is assigned to Intel Corporation.

2. This declaration is to establish conception of the invention in the above-identified application in the United States, at a date prior to August 31, 1999, the filing date of U.S. Patent No. 6,208,519, which was cited by the Examiner.

3. We understand that the invention relates to the following:

A. A method for assembling an integrated circuit package, comprising:

applying a thermal epoxy to a top surface of an integrated circuit;

placing a thermal element adjacent to the thermal epoxy;

curing the thermal epoxy with energy at a microwave frequency; and

applying an encapsulant over the integrated circuit, the thermal element and the thermal epoxy after curing of the thermal epoxy.

B. A method for assembling an integrated circuit package, comprising:

applying a thermal epoxy to a thermal element, the thermal epoxy being an epoxy resin contain a thermally conductive filler;

placing the thermal epoxy and the thermal element onto a top surface of an integrated circuit;

curing the thermal epoxy with energy at a microwave frequency; and

applying an encapsulant over the integrated circuit, the thermal element and the thermal epoxy after curing of the thermal epoxy to form the integrated circuit package.

C. A method comprising:

applying a thermal epoxy to a thermal element;

mounting the thermal element on a top surface of an integrated circuit placed in an integrated circuit package mounted on a substrate, the thermal epoxy interposed between the thermal element and the integrated circuit;

baking the substrate along with the integrated circuit package, the thermal element and the thermal epoxy; and

curing the thermal epoxy by radiating energy at a microwave frequency toward the thermal epoxy to cure the thermal epoxy without damaging the integrated circuit or heating other components of the integrated circuit package.

4. Prior to August 31, 1999, we completed an Intel Invention Disclosure (Exhibit A) describing the invention and submitted the invention disclosure to the legal department of Intel Corporation.

5. After receipt and review of the Intel Invention Disclosure, the legal department of Intel Corporation decided to proceed and requested Blakely, Sokoloff, Taylor & Zafman LLP to prepare and file a patent application on the subject matter set forth in Exhibit A.

6. Thereafter, the above-identified patent application was prepared with due diligence and filed on December 30, 1999.

We hereby declare that all statements made herein of my own knowledge are true and that the statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 6/1/04

Nagesh Vodrahalli

Date: 6/1/04

Biswajit Sur

EXHIBIT A

Redacted Copy of Invention Disclosure

INTEL CONFIDENTIAL P6785

TMG / TMG / Pckg
Thermomechanical
Com

TMG INVENTION DISCLOSURE, Rev 1, [redacted]

Located at: http://legal.intel.com

[redacted]

LEGAL ID# [redacted] (legal dept. use only) DATE: Invention Date: [redacted]

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444**.

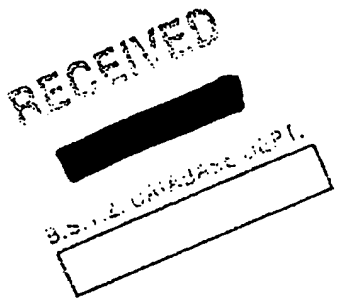
Fill out the below and follow the instructions:

1. **Field of the Invention:**

Semiconductor Process: device and integration
Semiconductor Process + Equipment: thin films
Semiconductor Process + Equipment: etch/litho
Circuit Design
Flash
Test
CQN (Q&R)
X Packaging
Boards/Cartridge
Automation
Other

2. **Concise Title of Invention:**

High performance thermal interface curing process for organic flip chip packages



3. Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):

The invention is: A curing process for the thermal interface material for organic flip chip packages (also known as C4 OLGA) that will result in a controlled bondline thickness without any resin seaparation or delamination. The invnetion helps maintain the warpage of the die constant during the entire curing process.

Description:

Problem: Organic flip chip packages typically have die warpage that varies as a function of die size and more importantly as a function of temperature. The thermal power dissipation demands are increasing with every generation of CPU products, and require a highly conductive thermal interface. The material thermal performance and the bondline control are critical elements in achiving such performance.

Silver filled epoxies are a class of materials that can provide the high thermal conductivity, For flip chip pakckges, the thermal epoxy is dispensed on the backside of the die, a heat spreader is placed with a known spring loading, and the whole assembly is cured in a conventional oven. Because of the warpage dependency with temperature, during the cure cycle, package and the die warpage change (become flattened). This provides a pumping action that results in either resin seaparation, or delamination (spreader to die) resulting in high thermal resistance of the interface.

Solution: The solution can be provided by maintaining the warpage of the whole assembly (spreader and the chip/package) dynamically same which is very difficult given different thermomechanical properties of the materials involved. The following method provides a practical solution for the problem.

The method employs the use of a variable frequency microwave curing to cure the thermal epoxy that is at the interface of the warped die and the flat spreader. The microwave curing will reduce the heating of the spreader and the more importantly the package assembly, therefore maintaining warpage change toa minimum during the cure. This therefore will eliminate the eliminate the resin seaparation and delamination issues during the cure, and giving the necessary high thermal performance of the interface.

The microwave curing frequencies are to be tailored for the curing of the specific epoxy to maximize the benefit. Microwave curing is being evaluated for the curing of the epoxy underfill for the C4 organic packageat Intel; results indicate that because of the variable frequency employed by the microwave curing tool, there is no damage to the electircal devices on the die (work in progress).

4. Inventor(s):

Name: Nagesh Vodrahalli | SS# [redacted] | Empl.# [redacted] | M/S: [redacted]
Phone: [redacted] | Fax: [redacted] | Home Address: [redacted]
Citizenship: [redacted] | Supervisor Name: [redacted] | Supervisor Phone: [redacted] | Supervisor M/S: [redacted]
Group Name: TMG | BUM Presenter: | Inventor Signature:
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN ___
SMTD____TCAD___
Other?_____

Name: Biswajit Sur | SS# [redacted] | Empl.# [redacted] | M/S [redacted]
Phone: [redacted] | Fax: [redacted] | Home Address: [redacted]
Citizenship: India | Supervisor Name: [redacted] | Supervisor Phone: [redacted] | Supervisor M/S: [redacted]
Group Name: TMG | BUM Presenter: | Inventor Signature:
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN ___
SMTD____TCAD___
Other?_____

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. *HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)*

DATE: _____ **SUPERVISOR NAME:** _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?**
If yes, explain and give date: [redacted]
(Give expected tape out date if applicable):

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel?** [redacted]
If yes, explain and give date:

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
If yes, explain and give date: [redacted]

9. **Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number:** [redacted]